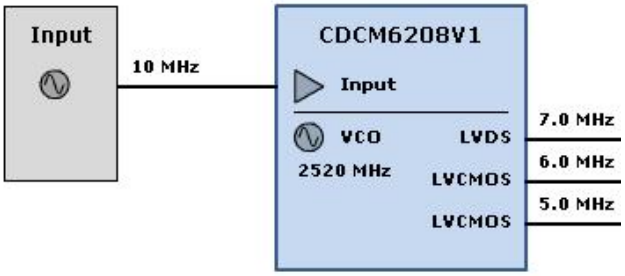
WEBENCH® Clock Architect

Project Report

Project: 4427995/1 Project 1 - [CDCM6208V1]
Created: 7/15/15 11:46:51 PM



Block Diagram

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	5	Any	1
fixed1	6	Any	1
fixed2	7	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	No

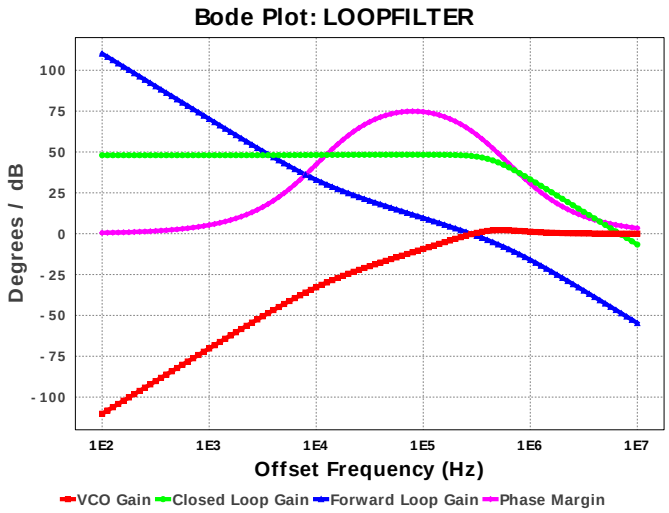
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$5.2
Total Current	132.5 mA
Total Footprint	49.0 mm^2

User ID = 4427995
Design Id = 17
Device = CDCM6208V1
Created = 7/15/15 11:46:51 PM

WEBENCH® Clock Design Report

Loop Filter: CDCM6208V1 LOOPFILTER



Preferences

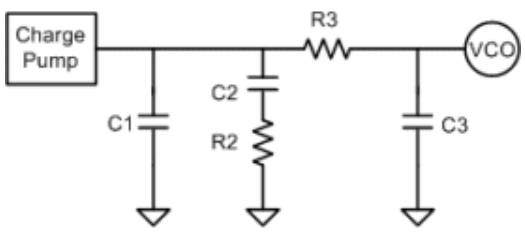
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.50 mA
VCO Gain	185.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2520.00 MHz
Phase Det. Frequency	10.00 MHz

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	292.129 kHz	N	277.417 kHz
Phase Margin	65.00 deg	N	63.223 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	9.50	N	11.963

Loop Filter Components

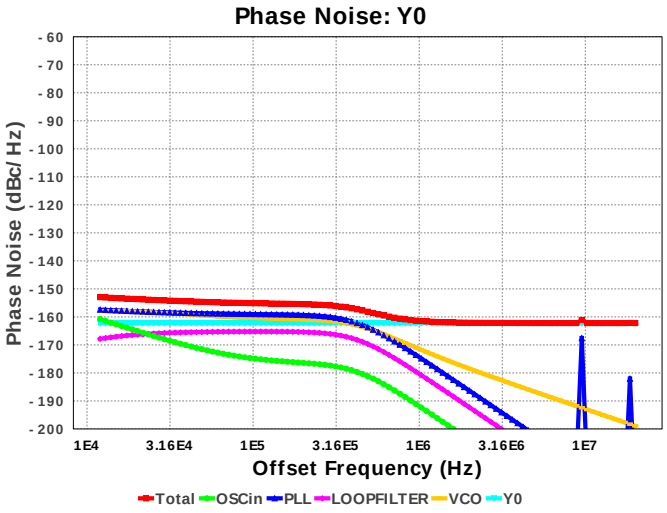
Name	Target Value	Fixed	Forced
C1	Open	N	N
C2	15.00 nF	N	N
C3	0.242 nF	Y	N
C4	Open	Y	N
R2	1.00 kohms	N	N
R3	0.10 kohms	Y	N



Output Block: CDCM6208V1 Y0 as LVDS output, 7.0 MHz

Integrated Noise Info 12000.0 - 2.0E7

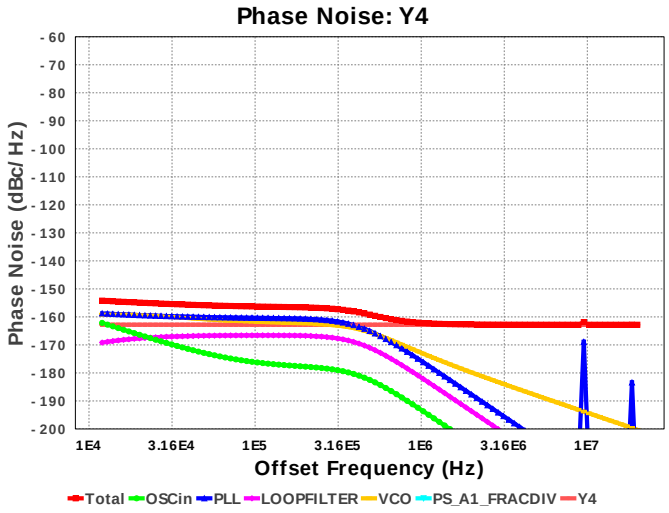
Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-161.734 dBc/Hz
RMS Jitter	1177.406 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.052 mrad
EVM	0.005%
SNR	85.716 dB
Spur	-88.716 dBc
Jitter (Pk-Pk)	8395.484 fs
Jitter (Cycle to Cycle Pk)	16790.969 fs
Jitter (Cycle to Cycle RMS)	1665.103 fs
A/D ENOB	13.953 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz



Output Block: CDCM6208V1 Y4 as LVCMOS output, 6.0 MHz

Integrated Noise Info 12000.0 - 2.0E7

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-162.404 dBc/Hz
RMS Jitter	1271.709 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.048 mrad
EVM	0.005%
SNR	86.386 dB
Spur	-89.386 dBc
Jitter (Pk-Pk)	9067.914 fs
Jitter (Cycle to Cycle Pk)	18135.829 fs
Jitter (Cycle to Cycle RMS)	1798.468 fs
A/D ENOB	14.064 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz



Output Block: CDCM6208V1 Y5 as LVCMOS output, 5.0 MHz

Integrated Noise Info 12000.0 - 2.0E7

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-162.521 dBc/Hz
RMS Jitter	1505.576 fs
RMS Phase Error (deg)	0.003 deg
RMS Phase Error	0.047 mrad
EVM	0.005%
SNR	86.503 dB
Spur	-89.503 dBc
Jitter (Pk-Pk)	10735.503 fs
Jitter (Cycle to Cycle Pk)	21471.006 fs
Jitter (Cycle to Cycle RMS)	2129.206 fs
A/D ENOB	14.084 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz